IN THE CLAIMS:

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6. (currently amended) A bi-directional level shifter for shifting a low voltage digital signal to a high voltage digital signal and vice-versa, the bi-directional level shifter comprising:

a first I/O terminal for sending and receiving the low voltage digital signal, the first I/O terminal receiving the low voltage digital signal ~~as an input~~ when the bi-directional level shifter shifts the low voltage digital signal to the high voltage digital signal, and the first I/O terminal sending the low voltage digital signal ~~as an output~~ when the bi-directional level shifter shifts the high voltage digital signal to the low voltage digital signal;

a second I/O terminal for sending and receiving the high voltage digital signal, the second I/O terminal receiving the high voltage digital signal ~~as an input~~ when the bi-directional level shifter shifts the high voltage digital signal to the low voltage digital signal, and the second I/O terminal sending the high voltage digital signal ~~as an output~~ when the bi-directional level shifter shifts the low voltage digital signal to the high voltage digital signal;

a first circuit operating at a low power supply voltage, the circuit comprising:

a first PMOS transistor having a source connected to the low power supply voltage;

a second PMOS transistor having a source connected to the low power supply voltage and a drain connected to the first I/O terminal;

a first NMOS transistor having a drain connected to a gate of the second PMOS transistor and a drain of the first PMOS transistor, a source connected to a reference voltage, and a gate connected to the second I/O terminal;

a second NMOS transistor having a drain connected to a gate of the first PMOS transistor and the drain of the second PMOS transistor, and a source connected to the reference voltage; and

a first inverter having an input connected to the second I/O terminal for receiving the high power digital signal, and an output connected to a gate of the second NMOS transistor; and

a second circuit operating at a high power supply voltage, the second circuit comprising:

a third PMOS transistor having a source connected to the high power supply voltage;

a fourth PMOS transistor having a source connected to the high voltage digital signal, and a drain connected to the second I/O terminal;

a third NMOS transistor having a source connected to a reference voltage, a drain connected to a gate of the fourth PMOS transistor and the drain of the third PMOS transistor, and a gate connected to the first I/O terminal;

a fourth NMOS transistor having a source connected to the reference voltage, and a drain connected to a gate of the third PMOS transistor and the drain of the fourth PMOS transistor; and

a second inverter having an input connected to the first I/O terminal for receiving the low voltage digital signal, and an output connected to a gate of the fourth NMOS transistor.

7. (original) The bi-directional level shifter according to claim 6, wherein the first circuit further comprises:

a fifth PMOS transistor having a gate connected to the gate of the second NMOS transistor, a source connected to the drain of the second PMOS transistor, and a drain connected to the drain of the second NMOS transistor; and

a fifth NMOS transistor having a drain connected to the first I/O terminal, a gate connected to the gate of the second NMOS transistor, and a source and a bulk connected to the reference voltage.

8. (original) The bi-directional level shifter according to claim 6, wherein the second circuit further comprises:

a sixth PMOS transistor having a gate connected to the gate of the fourth NMOS transistor, a source connected to the drain of the fourth PMOS transistor, and a drain connected to the drain of the fourth NMOS transistor; and

a sixth NMOS transistor having a drain connected to the second I/O terminal, a gate connected to the gates of the fourth NMOS transistor and the sixth PMOS transistor, and a source and a bulk connected to the reference voltage.

9. (currently amended) A bi-directional level shifter for shifting a low voltage digital signal to a high voltage digital signal and vice versa, the bi-directional level shifter comprising:

a first I/O terminal for sending and receiving the low voltage digital signal, the first I/O terminal receiving the low voltage digital signal ~~as an input~~ when the bi-directional level shifter shifts the low voltage digital signal to the high voltage digital signal, and the first I/O terminal sending the low voltage digital signal ~~as an output~~ when the bi-directional level shifter shifts the high voltage digital signal to the low voltage digital signal;

a second I/O terminal for sending and receiving the high voltage digital signal, the second I/O terminal receiving the high voltage digital signal ~~as an input~~ when the bi-directional level shifter shifts the high voltage digital signal to the low voltage digital signal, and the second I/O terminal sending the high voltage digital signal ~~as an output~~ when the bi-directional level shifter shifts

the low voltage digital signal to the high voltage digital signal;

a first circuit operating at a low power supply voltage, the circuit comprising:

a first PMOS transistor having a source connected to the low power supply voltage;

a second PMOS transistor having a source connected to the low power supply voltage and a drain connected to the first I/O terminal;

a first NMOS transistor having a drain connected to a gate of the second PMOS transistor and a drain of the first PMOS transistor, a source connected to a reference voltage, and a gate connected to the second I/O terminal;

a second NMOS transistor having a drain connected to a gate of the first PMOS transistor and the drain of the second PMOS transistor, and a source connected to the reference voltage;

a first inverter having an input connected to the second I/O terminal for receiving the high voltage digital signal, and an output connected to a gate of the second NMOS transistor;

a fifth PMOS transistor having a gate connected to the gate of the second NMOS transistor, a source connected to the drain of the second PMOS transistor, and a drain connected to the drain of the second NMOS transistor; and

a fifth NMOS transistor having a drain connected to the first I/O terminal, and a gate connected to the gate of the second NMOS transistor; and

a second circuit operating at a high power supply voltage, the second circuit comprising:

a third PMOS transistor having a source connected to the high power supply voltage;

a fourth PMOS transistor having a source connected to the high power supply voltage, and a drain connected to the second I/O terminal;

a third NMOS transistor having a source connected to a reference voltage, a drain connected to a gate of the fourth PMOS transistor and the drain of the third PMOS transistor, and a gate connected to the first I/O terminal;

a fourth NMOS transistor having a source connected to the reference voltage, and a drain connected to a gate of the third PMOS transistor and the drain of the fourth PMOS transistor;

a second inverter having an input connected to the first I/O terminal for receiving the low voltage digital signal, and an output connected to a gate of the fourth NMOS transistor;

a sixth PMOS transistor having a gate connected to the gate of the fourth NMOS transistor, a source connected to the drain of the fourth PMOS transistor,

and a drain connected to the drain of the fourth NMOS transistor; and

a sixth NMOS transistor having a drain connected to the second I/O terminal, a gate connected to the gates of the fourth NMOS transistor and the sixth PMOS transistor, and a source and a bulk connected to the reference voltage.

10. (Withdrawn) A bi-directional level shifter for shifting a low voltage digital signal to a high voltage digital signal and vice versa, the bi-directional level shifter comprising:

a first I/O terminal for sending and receiving the low voltage digital signal, the first I/O terminal receiving the low voltage digital signal as an input when the bi-directional level shifter shifts the low voltage digital signal to the high voltage digital signal, and the first I/O terminal sending the low voltage digital signal as an output when the bi-directional level shifter shifts the high voltage digital signal to the low voltage digital signal;

a second I/O terminal for sending and receiving the high voltage digital signal, the second I/O terminal receiving the high voltage digital signal as an input when the bi-directional level shifter shifts the high voltage digital signal to the low voltage digital signal, and the second I/O terminal sending the high voltage digital signal as an output when the bi-directional level shifter shifts the low voltage digital signal to the high voltage digital signal;

a first circuit operating at a low power supply voltage, the circuit comprising:

a first PMOS transistor having a source connected to the low power supply voltage;

a second PMOS transistor having a source connected to the low power supply voltage and a drain connected to the first I/O terminal;

a first NMOS transistor having a drain connected to a gate of the second PMOS transistor, and a source connected to a first reference voltage;

a second NMOS transistor having a drain connected to a gate of the first PMOS transistor, and a source connected to the first reference voltage;

a first inverter having an input connected to the second I/O terminal for receiving the high voltage digital signal, and an output;

a fifth PMOS transistor having a gate connected to the gate of the second NMOS transistor, a source connected to the drain of the second PMOS transistor, and a drain connected to the drain of the second NMOS transistor;

a fifth NMOS transistor having a drain connected to the first I/O terminal, a source connected to the first reference voltage, and a gate connected to the drain of the first PMOS transistor;

a seventh NMOS transistor having a gate connected to the first I/O terminal, a source connected to the

first reference voltage, and a drain connected to the drain of the first PMOS transistor;

a seventh PMOS transistor having a source connected to the drain of the first PMOS transistor, a drain connected to the drain of the first NMOS transistor, and a gate connected to a gate of the first NMOS transistor;

an eighth PMOS transistor having a source connected to the gate of the first NMOS transistor, a gate connected to the output of the first inverter, and a drain connected to the input of the first inverter;

an eighth NMOS transistor having a drain connected to the gate of the first NMOS transistor, a gate connected to the drain of the first PMOS transistor, and a source connected to the first reference voltage;

a ninth PMOS transistor having a source connected to the output of the first inverter, a drain connected to the gates of the second NMOS transistor and the fifth PMOS transistor, and a gate connected to the input of the first inverter; and

a ninth NMOS transistor having a source connected to the first reference voltage, a drain connected to the gates of the second NMOS transistor and the fifth PMOS transistor, and a gate connected to the first I/O terminal; and

a second circuit operating at a high power supply voltage, the second circuit comprising:

a third PMOS transistor having a source connected to the high power supply voltage;

a fourth PMOS transistor having a source connected to the high power supply voltage, and a drain connected to the second I/O terminal;

a third NMOS transistor having a source connected to a second reference voltage, and a drain connected to a gate of the fourth PMOS transistor;

a fourth NMOS transistor having a source connected to the second reference voltage, and a drain connected to a gate of the third PMOS transistor;

a second inverter having an input connected to the first I/O terminal for receiving the low voltage digital signal, and an output;

a sixth PMOS transistor having a gate connected to a gate of the fourth NMOS transistor, a source connected to the drain of the fourth PMOS transistor, and a drain connected to the drain of the fourth NMOS transistor;

a sixth NMOS transistor having a drain connected to the second I/O terminal, a source connected to the second reference voltage, and a gate connected to a drain of the third PMOS transistor;

a tenth NMOS transistor having a gate connected to the second I/O terminal, a source connected to the

second reference voltage, and a drain connected to the drain of the third PMOS transistor;

a tenth PMOS transistor having a source connected to the drain of the third PMOS transistor, a drain connected to the drain of the third NMOS transistor, and a gate connected to a gate of the third NMOS transistor;

an eleventh PMOS transistor having a source connected to the gate of the third NMOS transistor, a gate connected to the output of the second inverter, and a drain connected to the input of the second inverter;

an eleventh NMOS transistor having a drain connected to the gates of the third NMOS transistor and the tenth PMOS transistor, a source connected to the second reference voltage, and a gate connected to the drain of the third PMOS transistor;

a twelfth PMOS transistor having a source connected to the output of the second inverter, a drain connected to the gates of the fourth NMOS transistor and the sixth PMOS transistor, and a gate connected to the input of the second inverter; and

a twelfth NMOS transistor having a source connected to the second reference voltage, a drain connected to the gates of the fourth NMOS transistor and the sixth PMOS transistor, and a gate connected to the second I/O terminal.

11. (Withdrawn) The level shifter of claim 10, wherein the first inverter is coupled between the high power supply voltage and the second reference voltage and the second inverter is coupled between the low power supply voltage and the first reference voltage.

12. (Withdrawn) The level shifter of claim 11, wherein a bulk of the fifth PMOS transistor is connected to the low power supply voltage, a bulk of the seventh PMOS transistor is connected to the low power supply voltage, a bulk of the eighth PMOS transistor is connected to the high power supply voltage, and a bulk of the ninth PMOS transistor is connected to the high power supply voltage.

13. (Withdrawn) The level shifter of claim 12, wherein a bulk of the sixth PMOS transistor is connected to the high power supply voltage, a bulk of the tenth PMOS transistor is connected to the high power supply voltage, a bulk of the eleventh PMOS transistor is connected to the low power supply voltage, and a bulk of the twelfth PMOS transistor is connected to the low power supply voltage.

14. (Withdrawn) A single ended level shifter for shifting an input digital signal operating between first and second operating parameters to an output digital signal operating between third and fourth operating parameters that are different from the first and second operating parameters, the single ended level shifter comprising:

an input terminal receiving the input digital signal;

an output terminal for providing the output digital signal;

a first PMOS transistor having a source connected to a high power supply voltage;

a second PMOS transistor having a source connected to the high power supply voltage, and a drain connected to the output terminal;

a first NMOS transistor having a source connected to a first reference voltage, and a drain connected to a gate of the second PMOS transistor;

a second NMOS transistor having a source connected to the first reference voltage, and a drain connected to a gate of the first PMOS transistor;

an inverter having an input connected to the input terminal for receiving the input digital signal, and an output, wherein the inverter is coupled between a low power supply voltage and a second reference potential;

a third PMOS transistor having a source connected to the drain of the second PMOS transistor, a drain connected to the drain of the second NMOS transistor, and a gate connected to a gate of the second NMOS transistor;

a third NMOS transistor having a source connected to the first reference voltage, a drain connected to the output terminal, and a gate connected to drain of the first PMOS transistor;

a fourth PMOS transistor having a source connected to the drain of the first PMOS transistor, a drain connected to the drain of the first NMOS transistor, and a gate connected to a gate of the first NMOS transistor;

a fourth NMOS transistor having a source connected to the first reference voltage, a drain connected to the drain of the first PMOS transistor, and a gate connected to the output terminal;

a fifth PMOS transistor having a source connected to the gate of the first NMOS transistor, a drain connected to the input terminal, and a gate connected to the output of the inverter;

a fifth NMOS transistor having a source connected to the first reference voltage, a drain connected to the gate of the first NMOS transistor, and a gate connected to the drain of the first PMOS transistor;

a sixth PMOS transistor having a source connected to the output of the inverter, a drain connected to the gate of the second NMOS transistor, and a gate connected to the input of the inverter; and

a sixth NMOS transistor having a source connected to the first reference voltage, a drain connected to the gate of the second NMOS transistor, and a gate connected to the output terminal.

15. (Withdrawn) The level shifter of claim 14, wherein a bulk of the third PMOS transistor is connected to the high power supply voltage, a bulk of the fourth PMOS transistor is connected to the high power supply voltage, a bulk of the fifth PMOS transistor is connected to the low power supply voltage, and a bulk of the sixth PMOS transistor is connected to the low power supply voltage.